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Amendments to the Claims

1. (*Currently Amended*) Method of producing at least one semiconductor element in a semiconductor substrate, the semiconductor element having a plurality of cell types, the method comprising:

[[-]] producing at least one test structure on said semiconductor substrate, comprising a predetermined number of test cells having cell types similar to one or more of said plurality of cell types;

[[-]] each of said cell types having at least a first and a second local interconnect layer structure to be connected to predetermined supply voltages during use, a plurality of first and second polysilicon layer structures to provide control voltages to first and second electronic component structures, respectively;

[[-]] connecting in said test structure all of said plurality of said first polysilicon layer structures to one another to provide an interconnected first polysilicon layer structure, and connecting in said test structure all of said plurality of said second polysilicon layer structures to one another to provide an interconnected second polysilicon layer structure;

[[-]] providing predetermined test voltages to said first and second local interconnect layer structures, and to said interconnected first and second polysilicon layer structures, respectively;

[[-]] measuring currents resulting from said test voltages to identify production errors.

2. (*Original*) Method according to claim 1, wherein said plurality of said first and second polysilicon layer structures are connected to one another using metal connection structures.

3. (*Currently Amended*) Method ~~according to claim 1 or 2,~~ according to claim 1, wherein said test structure comprises CMOS transistors.

4. (*Currently Amended*) Method ~~according to any of the preceding claims,~~ according to claim 1, wherein said test voltages are selected such that at least one of the following production errors may be determined:

[[-]] one or more electrical shorts between said first and second polysilicon layer structures;

[[-]] one or more electrical shorts between at least one of said first and second local interconnect layer structures and at least one of said first and second polysilicon layer structures;

[[-]] n-gate oxide leakages;

[[-]] p-gate oxide leakages.

5. (*Currently Amended*) Method ~~according to any of the preceding claims,~~ according to claim 1,wherein said at least one semiconductor element is located in one of a plurality of reticles on a semiconductor wafer.

6. (*Currently Amended*) ~~A semiconductor substrate comprising at least one semiconductor element, the semiconductor element having a plurality of cell types, and at least one test structure comprising a predetermined number of test cells having cell types similar to one or more of said plurality of cell types, each of said cell types having at least a first and a second local interconnect layer structure to be connected to predetermined supply voltages during use, a plurality of first and second polysilicon layer structures to provide control voltages to first and second electronic component structures, respectively, in said test structure all of said plurality of said first polysilicon layer structures being connected to one another to provide an interconnected first polysilicon layer structure, and in said test structure all of said plurality of said second polysilicon layer structures being connected to one another to provide an interconnected second polysilicon layer structure.~~

A semiconductor substrate comprising at least one semiconductor element,

the semiconductor element having a plurality of cell types, and

at least one test structure comprising

a predetermined number of test cells having cell types similar to one or more of said plurality of cell types,

each of said cell types having at least a first and a second local interconnect layer structure to be connected to predetermined supply voltages during use,

a plurality of first and second polysilicon layer structures to provide control voltages to first and second electronic component structures, respectively, in said test structure all of said plurality of said first polysilicon layer structures being connected to one another to provide an interconnected first polysilicon layer structure, and

in said test structure all of said plurality of said second polysilicon layer structures being connected to one another to provide an interconnected second polysilicon layer structure.

7. (*Original*) A semiconductor device comprising a substrate according to claim 6.